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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/716,545	11/20/2000	Gajendra P. Singh	03226.049001;P5243	7006

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EXAMINER	
DONAGHUE, LARRY D	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/716,545	SINGH ET AL.	
	Examiner	Art Unit	
	Larry D. Donaghue	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/14/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-17 and 19-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-22,25 and 35-41* is/are rejected.

7)☒ Claim(s) *23,24,and 26-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1,2,4-17and 19-41 are presented for examination.

2. Claims 23, 24 and 26-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. The rejection is maintained and set forth below.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1,2, 4-17, 19-22, 25 and 35-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Joy et al. (6,507,862).

Joy et al. taught the invention as claimed including a system for implementing vertical threading in a processor, comprising: a header block that receives a multi-function signal (412) and generates a plurality of signals using the multi-function signal; and a data storage block (414) that is responsive to the plurality of signals generated by the header block and the multi-function signal comprises a scan enable function, a clock enable function, and a clock disable function (col. 10, lines 41-67).

As to claim 2, Joy et al. taught the header block comprises header circuitry which distinguishes between different functionalities exhibited by the multi-function signal (col. 10, lines 41-67).

As to claim 4, Joy et al. taught the header block receives signals in addition to the multi-function signal (col.10, lines 41-67).

As to claim 5, Joy et al. taught the additional signals received by the header block comprise a clock input signal and a global thread identifier signal (col. 10, lines 41-67).

As to claim 6, Joy et al. taught the global thread identifier signal is used by the processor to selectively indicate to the header block that the data storage block needs to switch process threads (Fig. 6, col. 15, line 52 – col. 17, line 32) .

As to claim 7, Joy et al. taught the clock input signal is generated by the processor and is used by the header block to determine time references for operations in the header block (col. 10, lines 41-67).

As to claim 8, Joy et al. taught the plurality of signals generated by the header block comprise an external pulse signal, an inverted external pulse signal, a scan clock signal, and a local thread identifier signal (col. 10, lines 41-67).

As to claim 9, Joy et al. taught the external pulse signal is used by the data storage block as a time reference for operations in a normal mode (col. 10, lines 41-67).

As to claim 10, Joy et al. taught the inverted external pulse signal is an inverse of the external pulse signal, and wherein the inverted external pulse signal is used by the data storage block to facilitate operations in a normal mode (col. 10, lines 41-67).

As to claim 11, Joy et al. taught the scan clock signal is used by the data storage block as a time reference for operations in a scan mode (col. 10, lines 41-67).

As to claim 12, Joy et al. taught, wherein the local thread identifier signal is generated by the header block using a global thread identifier signal (col. 10, lines 41-67).

As to claim 13, Joy et al. taught the data storage block receives the plurality of signals generated by the header block, and wherein the header block and the data storage block are part of a multiple-bit flip-flop, and wherein the multiple-bit flip-flop is used in a processor pipeline (410 and fig. 3).

As to claim 14, Joy et al. taught the processor pipeline comprises a plurality of multiple-bit flip-flops (col. 10, lines 41-67).

As to claim 15, Joy et al. taught the data storage block comprises at least one data storage element that is capable of storing data for a plurality of process threads (col. 10, lines 41-67) .

As to claim 16, Joy et al. taught the header block controls a plurality of modes in which the data storage block may operate, and wherein the multi function signal comprises additional functions (col. 10, lines 41-67).

As to claim 17, Joy et al. taught implementing vertical threading, comprising: receiving a mufti-function signal in a header block; determining which function the mufti-function signal serves; generating signals within and from the

header block according to the determination; and operating a multiple-bit flip-flop in one of a plurality of operation modes dependent upon the determination of which function the mufti-function signal serves (fig. 4a, col. 10, lines 41-67) and the mufti-function signal can serve as a scan enable function, a clock enable function, and a clock disable function (fig. 4a, col. 10, lines 41-67).

As to claim 19, Joy et al. taught the signals generated from the header block are received by a data storage block (fig. 4a, col. 10, lines 41-67).

As to claim 20, Joy et al. taught the data storage block operates in one of the plurality of operation modes dependent upon the signals generated from the header block (fig. 4a, col. 10, lines 41-67).

As to claim 21, Joy et al. taught the determination of which mode to operate the multiple-bit flip-flop comprises: distinguishing between multiple characteristics of the multi-function signal; using the multi-function signal to generate intermediary signals; and using the intermediary signals to determine when the multiple-bit flip-flop should go into or remain in one of the plurality of operation modes (fig. 4a, col. 10, lines 41-67).

As to claim 22, Joy et al. taught wherein the intermediary signals are internal to the header block, and wherein the plurality of operation modes comprise a normal mode and a scan mode (fig. 4a, col. 10, lines 41-67).

As to claim 25 , Joy et al. taught inputting a first clock signal; inputting the multi-function signal; inputting a global thread identifier signal; and selectively generating an external pulse signal, a scan clock signal, and a local thread. identifier signal dependent upon the behavior of the pulse signal, the multi-function signal, and the global thread identifier signal (fig. 4a, col. 10, lines 41-67).

As to claim 35, Joy et al. taught converting an existing processor without vertical threading into a processor with vertical threading without changing an architectural layout of the existing processor (col. 2, line 56 – col. 3, line 13).

As to claim 36, Joy et al. taught means for inputting a clock signal; means for inputting a multi-function signal; means for inputting a global thread identifier signal; means for distinguishing between different functionalities of the multi-function signal to determine which of a plurality of functions the multi-function serves; and means for generating a plurality of signals based on the determination of which of the plurality of functions the multi function serves, the clock signal, and the global thread identifier signal (fig. 4a, col. 10, lines 41-67).

As to claim 37, Joy et al. taught the plurality of signals comprises an external pulse signal, an inverted external pulse signal, a scan clock signal, and a local thread identifier signal (fig. 4a, col. 10, lines 41-67).

As to claim 38, Joy et al. taught means for generating an internal pulse signal based on the behavior of the clock signal; means for using the internal pulse signal as a time reference for operations; means for using the

internal pulse signal to generate the external pulse signal; and means for using the internal pulse to generate the inverted external pulse signal (fig. 4a, col. 10, lines 41-67).

As to claim 39, Joy et al. taught means for deactivating the external pulse signal when the global thread identifier signal toggles; means for reactivating the external pulse signal at an end of a cycle in which the global thread identifier signal toggled; and means for using the global thread identifier signal to generate the local thread identifier signal (fig. 4a, col. 10, lines 41-67).

As to claim 40, Joy et al. taught means for deactivating the external pulse signal when the multi function signal begins to serve as a scan enable function; means for reactivating the external pulse signal dependent upon whether the multi-function signal stopped serving as a scan enable function before an end of a clock cycle in which the multi-function signal began serving as the scan enable function; and means for activating a scan clock signal when the multi-function signal serves as the scan enable function for more than one clock cycle (fig. 4a, col. 10, lines 41-67).

As to claim 41, Joy et al. taught means for activating an internal scan ready signal at a beginning of a clock cycle immediately following a previous clock cycle in which the multi-function signal began serving as a scan enable function; and means for deactivating the internal scan ready signal when the multi function signal stops serving as the scan enable function (fig. 4a, col. 10, lines 41-67).

6. Claims 1,2, 4-17, 19-22, 25 and 35-41 are rejected under 35 U.S.C. 102(a) as being anticipated by Joy et al. (WO 00/68780).

Joy et al. taught the invention as claimed including a system for implementing vertical threading in a processor, comprising: a header block that receives a multi-function signal (412) and generates a plurality of signals using the multi-function signal; and a data storage block (414) that is responsive to the plurality of signals generated by the header block and the multi-function signal comprises a scan enable function, a clock enable function, and a clock disable function (page 14, line 19 – page 15, line 5).

As to claim 2, Joy et al. taught the header block comprises header circuitry which distinguishes between different functionalities exhibited by the multi-function signal (page 14, line 19 – page 15, line 5).

As to claim 4, Joy et al. taught the header block receives signals in addition to the multi-function signal (page 14, line 19 – page 15, line 5).

As to claim 5, Joy et al. taught the additional signals received by the header block comprise a clock input signal and a global thread identifier signal (page 14, line 19 – page 15, line 5).

As to claim 6, Joy et al. taught the global thread identifier signal is used by the processor to selectively indicate to the header block that the data storage block needs to switch process threads (Fig. 6, page 20, line 21 – page 24, line 6) .

As to claim 7, Joy et al. taught the clock input signal is generated by the processor and is used by the header block to determine time references for operations in the header block (page 14, line 19 – page 15, line 5).

As to claim 8, Joy et al. taught the plurality of signals generated by the header block comprise an external pulse signal, an inverted external pulse signal, a scan clock signal, and a local thread identifier signal (page 14, line 19 – page 15, line 5).

As to claim 9, Joy et al. taught the external pulse signal is used by the data storage block as a time reference for operations in a normal mode (page 14, line 19 – page 15, line 5).

As to claim 10, Joy et al. taught the inverted external pulse signal is an inverse of the external pulse signal, and wherein the inverted external pulse signal is used by the data storage block to facilitate operations in a normal mode (page 14, line 19 – page 15, line 5).

As to claim 11, Joy et al. taught the scan clock signal is used by the data storage block as a time reference for operations in a scan mode (page 14, line 19 – page 15, line 5).

As to claim 12, Joy et al. taught, wherein the local thread identifier signal is generated by the header block using a global thread identifier signal (page 14, line 19 – page 15, line 5).

As to claim 13, Joy et al. taught the data storage block receives the plurality of signals generated by the header block, and wherein the header block and the data storage block are part of a multiple-bit flip-flop, and wherein the multiple-bit flip-flop is used in a processor pipeline (410 and fig. 3).

As to claim 14, Joy et al. taught the processor pipeline comprises a plurality of multiple-bit flip-flops (c page 14, line 19 – page 15, line 5).

As to claim 15, Joy et al. taught the data storage block comprises at least one data storage element that is capable of storing data for a plurality of process threads (page 14, line 19 – page 15, line 5) .

As to claim 16, Joy et al. taught the header block controls a plurality of modes in which the data storage block may operate, and wherein the multi function signal comprises additional functions (page 14, line 19 – page 15, line 5).

As to claim 17, Joy et al. taught implementing vertical threading, comprising: receiving a mufti-function signal in a header block; determining which function the mufti-function signal serves; generating signals within and from the header block according to the determination; and operating a multiple-bit flip-flop in one of a plurality of operation

modes dependent upon the determination of which function the mufti-function signal serves (fig. 4a, page 14, line 19 – page 15, line 5) and the mufti-function signal can serve as a scan enable function, a clock enable function, and a clock disable function (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 19, Joy et al. taught the signals generated from the header block are received by a data storage block (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 20, Joy et al. taught the data storage block operates in one of the plurality of operation modes dependent upon the signals generated from the header block (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 21, Joy et al. taught the determination of which mode to operate the multiple-bit flip-flop comprises: distinguishing between multiple characteristics of the multi-function signal; using the multi-function signal to generate intermediary signals; and using the intermediary signals to determine when the multiple-bit flip-flop should go into or remain in one of the plurality of operation modes (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 22, Joy et al. taught wherein the intermediary signals are internal to the header block, and wherein the plurality of operation modes comprise a normal mode and a scan mode (fig. 4a, col. 10, lines 41-67).

As to claim 25 , Joy et al. taught inputting a first clock signal; inputting the multi-function signal; inputting a global thread identifier signal; and selectively generating an external pulse signal, a scan clock signal, and a local thread. identifier signal dependent upon the behavior of the pulse signal, the multi-function signal, and the global thread identifier signal (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 35, Joy et al. taught converting an existing processor without vertical threading into a processor with vertical threading without changing an architectural layout of the existing processor (page 3, line 11 – page 4, line 14).

As to claim 36, Joy et al. taught means for inputting a clock signal; means for inputting a multi-function signal; means for inputting a global thread identifier signal; means for distinguishing between different functionalities of the multi-function signal to determine which of a plurality of functions the multi-function serves; and means for generating a plurality of signals based on the determination of which of the plurality of functions the multi function serves, the clock signal, and the global thread identifier signal (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 37, Joy et al. taught the plurality of signals comprises an external pulse signal, an inverted external pulse signal, a scan clock signal, and a local thread identifier signal (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 38, Joy et al. taught means for generating an internal pulse signal based on the behavior of the clock signal; means for using the internal pulse signal as a time reference for operations; means for using the

internal pulse signal to generate the external pulse signal; and means for using the internal pulse to generate the inverted external pulse signal (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 39, Joy et al. taught means for deactivating the external pulse signal when the global thread identifier signal toggles; means for reactivating the external pulse signal at an end of a cycle in which the global thread identifier signal toggled; and means for using the global thread identifier signal to generate the local thread identifier signal (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 40, Joy et al. taught means for deactivating the external pulse signal when the multi function signal begins to serve as a scan enable function; means for reactivating the external pulse signal dependent upon whether the multi-function signal stopped serving as a scan enable function before an end of a clock cycle in which the multi-function signal began serving as the scan enable function; and means for activating a scan clock signal when the multi-function signal serves as the scan enable function for more than one clock cycle (fig. 4a, page 14, line 19 – page 15, line 5).

As to claim 41, Joy et al. taught means for activating an internal scan ready signal at a beginning of a clock cycle immediately following a previous clock cycle in which the multi-function signal began serving as a scan enable function; and means for deactivating the internal scan ready signal when the multi function signal stops serving as the scan enable function (fig. 4a, page 14, line 19 – page 15, line 5).

7. Applicant's arguments filed 03/14/2006 have been fully considered but they are not persuasive.

As to applicant's arguments directed to claims 1 and 17, Applicant states Applicant argues in substance cited passages relied in Joy to fail to teach all the limitations in the claim and the cited passage and, in fact, the remainder of the reference are silent regarding the multi-function signal comprising a clock *disable* function, as required by the claim."

REPONSE

A clock enable function inherently includes a disable function all enable signal can be either off or on.

As to applicant arguments directed to claims 2 and 36, Applicant argues in substance cited passages relied upon to teach all the limitations, but the cited passage, and in fact, the remainder of the reference, are silent regarding a header circuitry, or any element distinguishing between different functionalities exhibited by the multi-function signal.

RESPONSE

The reference set forth that the multi-function signal is used to derive other signal therefore it functionality must be determined for the proper operation of the system.

As to applicant's argument directed to 9-11,16,20 and 22, Applicant argues in substance the cited passage relied upon to teach all the limitations of the claims 9-11,16,20 and 22, but the cited passage, and in fact, the

remainder of the reference, are silent regarding an external pulse signal being used as a time reference for operations in a normal mode. In fact, Joy never distinguishes normal mode from scan mode.

RESPONSE

The scan enable is required to change to scan mode, therefore the system must be in another operating state before the scam enable is applied, (normal mode).

Those claims not expressly argued are rejected for the same reasons as their parent claims.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Larry D. Donaghue whose telephone number is 571-272-3962. The examiner can normally be reached on M-F 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).